IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319 5940

International Journal of Advanced Research in Computer and Communication Engineering
ISO 3297:2007 Certified
Vol. 6, Issue 3, March 2017

Design of Reversible Excess-3 Adder and Subtractor

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Abstract: Power is one of the most important design parameter after speed, in integrated circuit. One of the basic fundamental component in such circuit is adder and subtractor. In order to optimize such circuits there is need of designing efficient and low power fundamental blocks. As per the Launder's principle, KTln2 heat is dissipated if there is any loss in bit. Excess-3 code is one of the sequential code used widely in digital circuits for performing arithmetic operations. Since conventional excess-3 adder and excess-3subtractor both circuits designed in irreversible logic observe large amount of leakage power. By keeping this as main point, this paper explains the process of designing 4-bit excess-3 adder and subtactor in 90nm technology and also worked to combine both individual circuit to design as a single circuit where it can perform addition and subtraction on excess-3 coded bits simultaneously. This paper also gives mathematical analysis of n-bit proposed circuit in terms of number of gates, quantum cost, garbage output, power and delay. Finally simulation results are obtained by using cadence virtuoso and observed power dissipation for proposed circuit is 171uW.In this paper detail simulation results along with the power graph submitted.

Keywords: Quantum Cost (QC), Garbage Outputs (GO), Fredkin gate (F), Peres Gate (PG), Feynman gate (FG), Reversible MUX(RMUX), Reversible full adder (RFA), Reversible Parallel adder, GSR logic cell.

1. INTRODUCTION

Addition and subtractions are the basic arithmetic operations used widely in digital technology. These operations are performed by Adder and Subtraction hardware which are present in ALU [1]. In order to add or subtract multiple bits by cascading several full adders. Subtraction operations are performed by adding two bits where one of the bit is 2's complement. Arithmetic operations are performed in three sequential codes i.e. binary codes, BCD code and excess-3 code, in this paper considered excess-3 code.

Excess-3 codes are considered as a non-weighted BCD code since it corresponds 8421 code word plus 0011(3). Since excess-3 code is self-complemented, subtraction operation can be performed easily than other codes. There are six invalid states in excess-3 code 0000, 0001, 0010, 1101, 1110, and 1111 [2]. By adding two bits of excess-3 codes raw sum is excess-6 code, so in order correct this, it suggested has to remove extra bias by adding 3 from the sum if decimal less than 10 and if decimal more than 10 have to subtract 3 form the sum. Since excess-3 adder and excess three subtractor designed using irreversible logic observe large amount of power dissipation.

According to Launder whenever a computer transmits data from the previous bits then certain amount of energy dissipated, in this case if there is any bit is lost then certain amount of power is leaked. In order to overcome this problem it is necessary to recover those bits which are lost. After having several analyses C.H. Bennett [3, 4] in 1973 concluded that there will be no energy dissipation when system travels from initial to final position. It means that in order to neglect power dissipation circuit must be designed using reversible gates. As a result Reversible logic is considered as efficient technique.

The design flow of Reversible excess-3 adder and subtractor explained in this paper is segregated into five sections. Section 2, discuss about existing work, Section 3, it explains proposed design. Section 4, it shows the simulation results of each and every circuit along with the power curve and shows separately overall power to imply power reduction. Section 5, mathematical analysis for n-Bit Reversible Exess-3 adder and subtractor. Section 6, conclusion.

2. EXISTING WORK

In designing any digital system using reversible logic number of gates, quantum cost and garbage outputs are major parameters for analyzing had defined in [5]. In this paper in section 5 above parameters are analyzed for proposed circuit.

As per the conventional excess 3 [2] adder and subtractor circuit clearly comes to know that still improvement can be done to optimize in terms of power. And also it is possible to design a single excess-3 based circuit for performing addition and subtraction.

In-order to perform excess-3 addition add the excess-3 number by segregating whole number into groups of each 4-bit number from LSB bit. Now observe the carry bit of each group, if carry = 1 add the sum with 0011 or if carry = 0 subtract 0011 from the sum since the obtained result will be in excess-6 format. Fig. 1 explains excess-3 adder architecture clearly. In-order to perform excess-3 subtraction, subtract the excess-3 number by segregating

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whole number into groups of each 4-bit number from LSB bit. Now observe the borrow of each group. If borrow=1, subtract 0011 from difference and if borrow=0, add 0011 to the difference. Fig. 2 explains detail architecture of excess-3 subtraction.

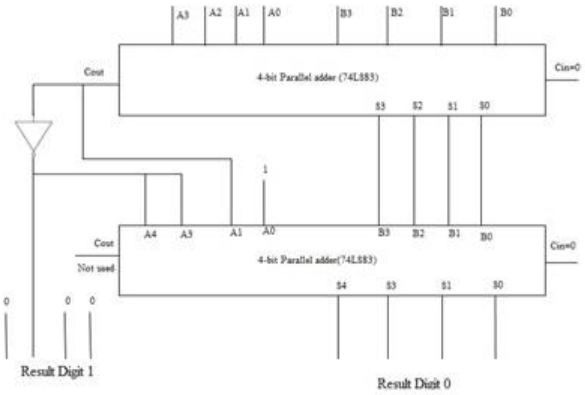

Fig. 1 Logic Diagram of 4-but excess-3 adder

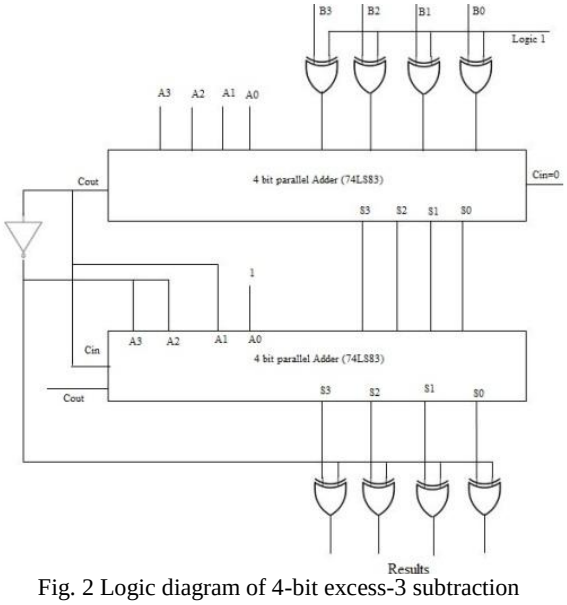

Fig. 2 Logic diagram of 4-bit excess-3 subtraction

This paper worked to design a single circuit which performs both addition and subtraction for this purpose reversible MUX is used from [6].

3. PROPOSED EXCESS-3 ADDER SUBTRACTOR

In order to design proposed circuit, there is need of designing the supporting circuitry in reversible logic. This paper consider [2] as its main reference.

3.1. Reversible Full Adder

Full adder calculates binary data and accounts for carried values in and out. It adds three bits and provides sum and carry. It can be designed in various styles, but in this paper full adder is designed in reversible logic using two PG gates. Simulation results of RFA are discussed in section 4. Fig. 3 explains detail RFA architecture.

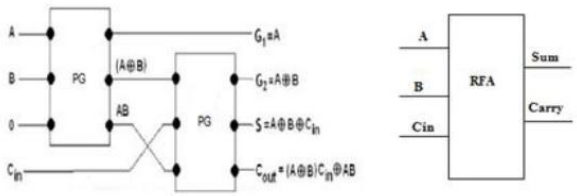

Fig. 3 Reversible Full Adder

3.2. Reversible Parallel Adder

It is possible to design logic to add n-bits by using multiple full adders where Cin of each full adder is Cout of previous full adder. Since it adds binary numbers in parallel form it is called as parallel Adder. In order to design 4-bit RPA, this paper cascades four RFA since required 4-bit RPA. Fig. 4 explains detail architecture of 4-bit RPA

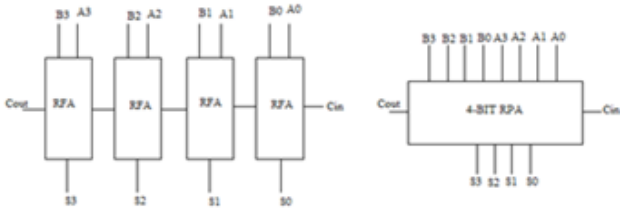

Fig. 4 Reversible 4-bit Reversible Parallel Adder

3.3. GSR logic cell

As per the conventional designs, there are two individual circuits to perform addition and subtraction of two excess-3 coded bits. By keeping this as criteria, this paper designed only one single circuit by combining two circuits. For this purpose this paper designed a special logic block i.e. GSR logic which can be triggered simultaneously to obtain addition and subtraction at a time which the controlling signal. In order to design GSR logic block, four FG gates and four reversible 2:1 MUX are used and the architecture is explained in Fig. 5. Operation of GSR logic block varies with control signal i.e. if control =1; it helps to operate excess-3 subtractor and if control = 0; it helps to operate excess-3 adder.

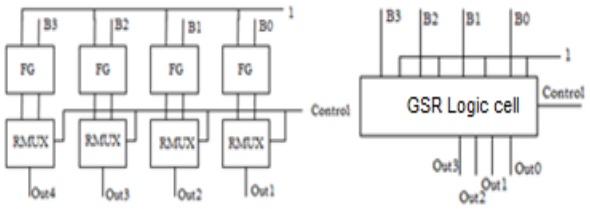

Fig. 5 4-bit GSR logic cell

3.4. Proposed 4-bit Reversible Excess-3 adder subtractor

In order to design proposed circuit, this paper used two GSR logic cell, two RPA, one FG gate and one RMUX. GSR logic cell enables to operate a proposed circuit in addition and subtraction mode with respect to control signal. First GSR logic gives required output O1, O2, O3, O4 by considering B0, B1, B2, B3 and 1 as a input with

IJARCCE

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ISSN (Print) 2319 5940

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respect control signal. And these outputs are considered as inputs for RPA and also consider A0, A1, A2, and A3 as other four inputs to calculate 4-bit sum and one bit carry. These outputs are feed as inputs to other RPA to correct the result form excess-6 format as this paper discussed in section 1. And finally one more GSR logic cell is used to trigger to get respective outputs as per the control signal. Fig. 6 explains detail architecture of 4-bit proposed reversible excess-3 adder and subtractor.

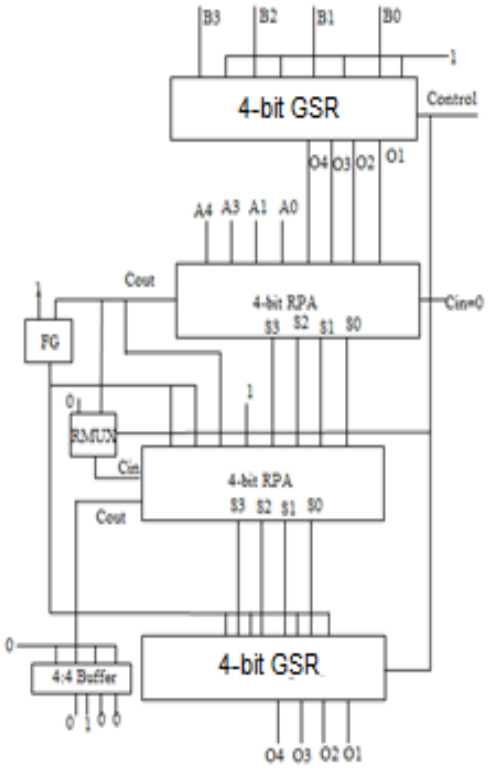

Fig. 6 4-bit Proposed Reversible Excess-3 adder and subtractor

4. SIMULATION RESULTS OF PROPOSED CIRCUIT

In these section simulation results of each and every reversible logic used in design is shown along with their power curve, this are obtained through cadence virtuoso.

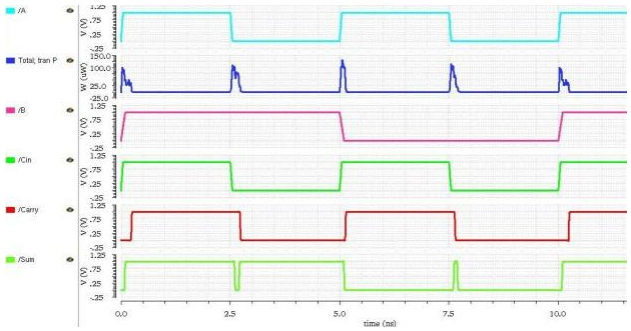

Fig. 7 Simulation result of 2-bit RFA when V_{dd} is 1V and power dissipation is 5.49uW

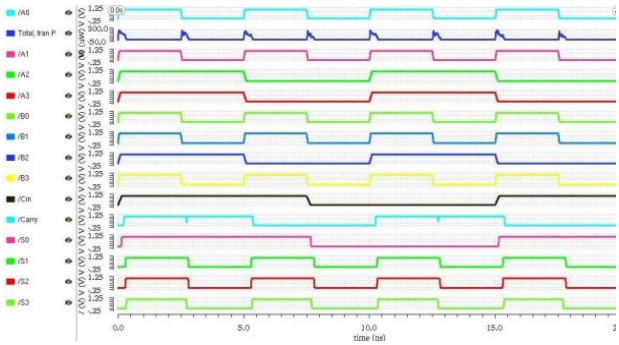

Fig. 8 Simulation result of 4-bit RPA when $V_{dd}$is 1V and power dissipation is 13.52uW

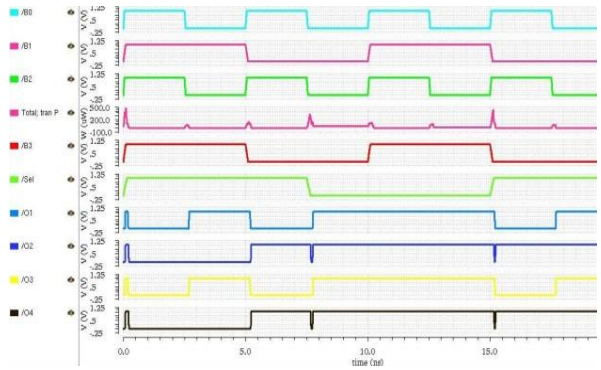

Fig. 9 Simulation result of GSR logic cell where V_{dd} is 1V and power dissipation is 14.23uW

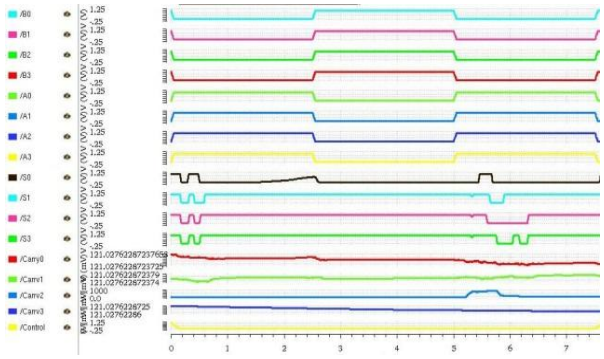

Fig. 10 Simulation result of proposed Reversible 4-bit excess-3 adder subtractor in addition mode by control signal is 0 where V_{dd} is 1V

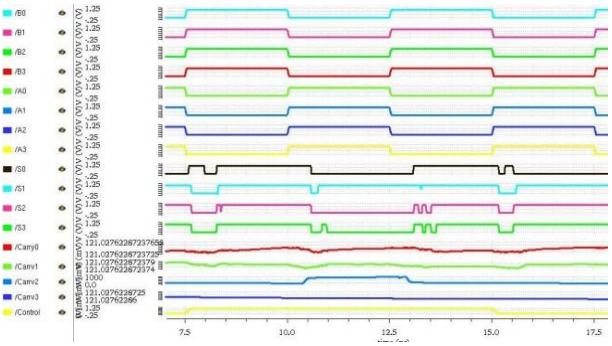

Fig. 11 Simulation result of proposed Reversible 4-bit excess-3 adder subtractor in subtraction mode by control signal is 1 where V_{dd} is 1V

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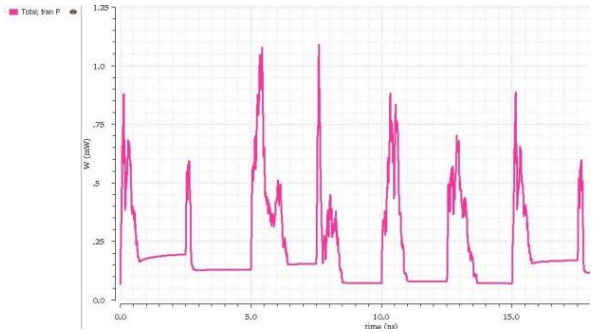

Fig. 12 Simulation result of proposed 4-bit excess-3 adder subtractor power dissipation curve calculated as 171uW

5. MATHEMATICAL ANALYSIS FOR N-BIT PROPOSED REVERSIBLE EXCESS-3 ADDER SUBTRACTOR

5.1. Number of Gates (NOG)

In order to calculate number of gates used, this paper count all gates used in individual cell. To design 4-bit RPA used four RFA where each one designed using two PG gates. To design 4-bit GSR logic cell used four RMUX where each one designed by F gate and four FG gates. And finally used one RMUX and one FG gate.To calculate NOG for n-bit proposed excess-3 adder subtractor following equation deduced

$NOGn\text{-}bit = 2n/4NOGRPA+2n/4NOG_{GSR}+NOG_{RMUX}+NOG_{FG}$

$= 2n/4[4\times NOG_{RFA}]+2n/4[NOG_{FG}+NOG_{RMUX}]+1+1$

$= 2n/4[4\times 2]+2n/4[4+4]+2$

$= 8n+2$ (1)

5.2. Garbage Output (GO)

Now, the total Garbage Output i.e. unused outputs, required for proposed n-bit reversible excess-3adder subtractor is given by the following expression

$GOn\text{-}bit = 2n/4GORPA+2n/4GO_{GSR}+GO_{RMUX}+GO_{FG}$

$= 2n/4[4\times GO_{RFA}]+2n/4[GO_{FG}+GO_{RMUX}]+2+1$

$= 2n/4[4\times 2]+2n/4[0+4\times 2]+3$

$= 8n+3$ (2)

5.3. Quantum Cost (QC)

The quantum cost for n-bit proposed reversible excess-3 adder subtractor is

$QCn\text{-}bit = 2n/4QCRPA+2n/4QC_{GSR}+QC_{RMUX}+QC_{FG}$

$= 2n/4[4\times QC_{RFA}]+2n/4[QC_{FG}+QC_{RMUX}]+5+1$

$= 2n/4[4\times 8]+2n/4[1+5]+6$

$= 19n+6$ (3)

5.4. Power

The total power for proposed n-bit reversible excess-3 adder subtractor is given by the following expression

$P_{n\text{-}bit} = 2n/4[4P_{RPA}]+2n/4[4P_{GSR}]+P_{RMUX}+P_{FG}$

With help of cadence virtuoso this paper calculated power for each and every individual logic block and observed as

$P_{4bitRPA}=13.52uW; P_{GSR}=14.23uW; P_{RMUX=}1.6uW; P_{FG}=1.2uW$

$Pn\text{-}bit = [2n[13.52]+2n[14.23]+1.6+1.2]\ uW$

$=[55.5n+1.8]\ uW$ (4)

5.5. Delay

Total delay for proposed n-bit reversible CSLA is given by the following expression

$Dn\text{-}bit = 2n/4[4DRPA]+2n/4[4D_{GSR}]+D_{RMUX}+D_{FG}$

With help of cadence virtuoso this paper calculated delay for each and every individual logic block and observed as $D_{4bitRPA}=0.27ns; D_{GSR}=0.186ns; D_{RMUX}=0.093ns; D_{FG}=0.034$ ns

$Dn\text{-}bit = [2n[0.27]+2n[0.186]+0.093+0.034]\ ns$

$= [0.912n+0.127]\ ns$ (5)

6. CONCLUSION

Power and Area are the main parameters while designing any VLSI circuits. This paper finally submits optimized reversible 4-bit excess-3 adder subtractor which consumes less power and less area by combining two separate circuits as whole single circuit. Proposed novel reversible excess-3 adder subtractor has number of gates, quantum cost, garbage output, power and delay are 8n+2, 8n+3, 19n+6, [55.5n+1.8] uW and [0.912n+0.127] ns respectively. Design and simulations are performed using cadence 90nm technology.

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